AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (Cancelled):

Claim 2 (Previously Presented):

The electronic circuit as recited in claim 3, wherein when the self-test detects that one of the slice arrays is defect free, the remap register associated with that slice array is set to indicate that the slice array is defect free resulting in the associated remap selector circuit instructing the associated write selector circuit to direct data intended for storage in that slice array to that slice array and instructing the associated read selector circuit to direct data read from that slice array to the output of that slice array.

Claim 3 (Previously Presented):

An electronic circuit for self-repair of a random access memory array, comprising:

a write selector circuit associated with each slice array, wherein the random access memory is organized into a plurality of slice arrays, wherein each slice array comprises at least one memory storage cell, and wherein at least one of the slice arrays is redundant;

a read selector circuit associated with each slice array;

a remap selector circuit associated with each slice array; and

a remap register associated with each slice array, wherein when power is applied to the circuit, the circuit automatically performs a self-test, wherein when the self-test detects a defect, the remap register of the slice array having the defect is set to indicate the presence of the defect resulting in the associated remap selector circuit instructing the associated write selector circuit to redirect data intended for storage in that slice array to an adjacent slice array and instructing the associated read selector circuit to redirect data read from the adjacent slice array to the output of the defective slice array, wherein the remap selector circuit associated with each slice array comprises an OR gate, wherein the OR gate has a first OR-gate input, a second OR-gate input, and an OR-gate output, wherein the first OR-gate input is connected to the OR-gate output associated with the adjacent higher-numbered slice array, wherein the second OR-gate input is connected to the output of

the remap register, and wherein the OR-gate output is connected to the input of the write selector circuit and the read selector circuit.

Claim 4 (Previously Presented):

An electronic circuit for self-repair of a random access memory array, comprising:

a write selector circuit associated with each slice array, wherein the random access memory is organized into a plurality of slice arrays, wherein each slice array comprises at least one memory storage cell, and wherein at least one of the slice arrays is redundant;

a read selector circuit associated with each slice array;

a remap selector circuit associated with each slice array; and

a remap register associated with each slice array, wherein when power is applied to the circuit, the circuit automatically performs a self-test, wherein when the self-test detects a defect, the remap register of the slice array having the defect is set to indicate the presence of the defect resulting in the associated remap selector circuit instructing the associated write selector circuit to redirect data intended for storage in that slice array to an adjacent slice array and instructing the associated read selector circuit to redirect data read from the adjacent slice array to the output of the defective slice array, wherein the write selector circuit associated with each slice array comprises a write multiplexer, wherein the write multiplexer has a first write-multiplexer input, a second write-multiplexer input, a write-multiplexer control input, and a write-multiplexer output, wherein the write-multiplexer control input is connected to the output of the remap selector circuit, wherein the first write-multiplexer input is connected to the second write-multiplexer input associated with the adjacent higher-numbered slice array, wherein the second write-multiplexer input is connected to an output of an input register, and wherein the write-multiplexer output is capable of transferring data to the slice array.

Claim 5 (Previously Presented):

An electronic circuit for self-repair of a random access memory array, comprising:

a write selector circuit associated with each slice array, wherein the random access memory is organized into a plurality of slice arrays, wherein each slice array comprises at least one memory storage cell, and wherein at least one of the slice arrays is redundant;

a read selector circuit associated with each slice array;

a remap selector circuit associated with each slice array; and

a remap register associated with each slice array, wherein when power is applied to the circuit, the circuit automatically performs a self-test, wherein when the self-test detects a defect, the remap register of the slice array having the defect is set to indicate the presence of the defect resulting in the associated remap selector circuit instructing the associated write selector circuit to redirect data intended for storage in that slice array to an adjacent slice array and instructing the associated read selector circuit to redirect data read from the adjacent slice array to the output of the defective slice array, wherein the read selector circuit associated with each slice array comprises a read multiplexer, wherein the read multiplexer has a first read-multiplexer input, a second read-multiplexer input, a read-multiplexer control input, and a read-multiplexer output, wherein the read-multiplexer control input is connected to the output of the remap selector circuit, wherein the first read-multiplexer input is capable of obtaining data from the slice array, wherein the second read-multiplexer input is connected to the first read-multiplexer input associated with the adjacent lowered-numbered slice array, and wherein the read-multiplexer output is capable of transferring data to an output register.

Claim 6 (Previously Presented):

The electronic circuit as recited in claim 3, wherein the electronic circuit is embedded within a bit-slice in an integrated circuit, wherein the bit-slice comprises the slice array and other circuitry associated with the slice array.

Claim 7 (Previously Presented):

The electronic circuit as recited in claim 3, wherein when the defect is present:

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the write selector circuit to redirect data intended for storage in that slice array to its adjacent slice array, and

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the read selector circuit to redirect data read from its adjacent slice array to the output of the slice array,

Claim 8 (Previously Presented):

The electronic circuit as recited in claim 3, wherein the electronic circuit is an integrated circuit.

Claim 9 (Cancelled):

Claim 10 (Previously Presented):

The electronic circuit as recited in claim 4, wherein when the self-test detects that one of the slice arrays is defect free, the remap register associated with that slice array is set to indicate that the slice array is defect free resulting in the associated remap selector circuit instructing the associated write selector circuit to direct data intended for storage in that slice array to that slice array and instructing the associated read selector circuit to direct data read from that slice array to the output of that slice array.

Claim 11 (Previously Presented):

The electronic circuit as recited in claim 4, wherein the electronic circuit is embedded within a bit-slice in an integrated circuit, wherein the bit-slice comprises the slice array and other circuitry associated with the slice array.

Claim 12 (Previously Presented):

The electronic circuit as recited in claim 4, wherein when the defect is present:

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the write selector circuit to redirect data intended for storage in that slice array to its adjacent slice array, and

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the read selector circuit to redirect data read from its adjacent slice array to the output of the slice array,

Claim 13 (Previously Presented):

The electronic circuit as recited in claim 4, wherein the electronic circuit is an integrated circuit.

Claim 14 (Previously Presented):

The electronic circuit as recited in claim 5, wherein when the self-test detects that one of the slice arrays is defect free, the remap register associated with that slice array is set to indicate that the slice array is defect free resulting in the associated remap selector circuit instructing the associated write selector circuit to direct data intended for storage in that slice array to that slice array and instructing the associated read selector circuit to direct data read from that slice array to the output of that slice array.

Claim 15 (Previously Presented):

The electronic circuit as recited in claim 5, wherein the electronic circuit is embedded within a bit-slice in an integrated circuit, wherein the bit-slice comprises the slice array and other circuitry associated with the slice array.

Claim 16 (Previously Presented):

The electronic circuit as recited in claim 5, wherein when the defect is present:

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the write selector circuit to redirect data intended for storage in that slice array to its adjacent slice array, and

for each slice array subsequent to the slice array in which the defect is present, the remap selector circuit instructs the read selector circuit to redirect data read from its adjacent slice array to the output of the slice array,

Claim 17 (Previously Presented):

The electronic circuit as recited in claim 5, wherein the electronic circuit is an integrated circuit.